REMARKS

Claims 1-37 are pending. The drawings have been amended. No new matter has been added. The Examiner's reconsideration of the rejections is respectfully requested in view of the above amendments and the following remarks.

Regarding the Amendments to Figures 1, 2 and 3, all of which used Reference Numeral 120 as the label for the CPU. The Specification, as filed, refers to the CPU as being identified by Reference Numeral 110. Thus, the figures have been amended to reflect the Specification.

Claim Rejections – 35 U.S.C. §112

Claim 3 stands rejected under 35 U.S.C. §112, for failing to comply with both the written description requirement and the enablement requirement for the reasons cited on pages 2 and 3 of the Office Action.

Claim 3, as amended, is believed to satisfy the requirements of 35 U.S.C. §112. Accordingly, withdrawal of the 35 U.S.C. §112 rejections is respectfully requested.

Claim Rejections – 35 U.S.C. §102

In accordance with the Office Action, Claims 1, 2, 4-8, 15-20, 22, 23, 25-34 and 37 stand rejected under 35 U.S.C. §102(e), for reasons stated on pages 3-7 of the office action, as being anticipated by US Patent 6,678,790 to Kumar, hereinafter Kumar. Applicants respectfully submit that at the very minimum Kumar fails to anticipate claims 1, 22, 26, 29, 30 and 33.

For example, applicants respectfully submit that Kumar does not teach or suggest *a configurable memory comprising a memory portion for storing tag bits and data bits in a single logical line, wherein the configurable memory is configured as a*

cache, as essentially claimed in Claims 1, 22, 26, 29, 30 and 33. In fact, with regard to the Office Action's arguments with respect to Claim 22 (on pages 3 and 4 of the Office Action), the Examiner did not explain, where and how the cited sections of Kumar teaches *a configurable memory comprising a memory portion for storing tag bits and data bits in a single logical line, wherein the configurable memory is configured as a cache* as essentially claimed. In any event, there is nothing in the cited sections of Kumar that discloses or suggests this feature. Thus, Kumar fails to teach every element of Claims 1, 22, 26, 29, 30 and 33. Therefore, Kumar fails to anticipate the above-cited Claims.

Applicants respectfully submit that at a minimum Claims 2-21, 23-25, 27, 28, 31, 32 and 34-37 are not anticipated by Kumar at least by virtue of their dependence from independent Claims 1, 22, 26, 29, 30 and 33 for at least the reasons stated above.

In accordance with the Office Action, Claims 1, 6, 9-14, 21 and 29 stand rejected under 35 U.S.C. §102(e), as being anticipated by US Patent 6,606,684 to Ramagopal et. al., hereinafter Ramagopal, for reasons cited on pages 7-10 of the Office Action. Applicants respectfully submit that at the very minimum, Ramagopal fails to anticipate Claims 1 and 29, since it does not teach or suggest *a configurable memory comprising a memory portion for storing tag bits and data bits in a single logical line, wherein the configurable memory is configured as a cache* as essentially claimed in Claims 1 and 29.

Claims 6, 9-14 and 21 depend from Claim 1. The dependent claims are patentable over Ramagopal at least by virtue of their dependence from Claim 1.

In accordance with the Office Action, Claim 12 stands rejected under 35 U.S.C. §102(e), as being anticipated by US Patent 6,321,318 to Baltz, hereinafter Baltz, for the

reasons given on pages 9-10 of the Office Action. Applicants respectfully submit that at the very minimum, Baltz fails to anticipate Claim 1, from which claim 12 depends, because Baltz does not teach or suggest *a configurable memory comprising a memory portion for storing tag bits and data bits in a single logical line, wherein the configurable memory is configured as a cache*, as essentially claimed in Claim 1.

Therefore, Baltz fails to anticipate Claim 12, at least by virtue of its dependence form Claim 1.

Accordingly, withdrawal of the anticipation rejections is respectfully requested.

Claim Rejections – 35 U.S.C. §103

In accordance with the Office Action the following claim rejections were asserted under 35 U.S.C. §103(a):

(i) Claim 3 stands rejected as being unpatentable over Kumar in view of US Patent 6,355,968 to Lehmann, hereinafter Lehmann, for reasons stated on page 10 and 11;

(ii) Claim 24 stands rejected as being unpatentable over Kumar in view of US Patent 6,377,912 to Sample, hereinafter Sample, or in the alternative in view of US Patent 6,611,796 to Natarajan, hereinafter Natarajan, for the reasons stated on page 11 of the Office Action;

(iii) Claims 34 and 35 stand rejected as being unpatentable over Kumar in view of US Patent 6,426,549 to Isaak, hereinafter Isaak, for the reasons stated on pages 11-12 of the Office Action.

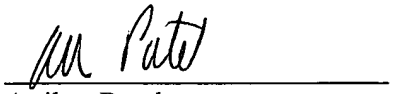
Each of the above rejections is based, in part, on the contention that Kumar teaches the elements of independent Claims 1, 22 and 33, from which Claims 3, 24, 34

and 35 respectfully depend. However, as Kumar, does not teach or suggest the inventions of Claims 1, 22 and 33, because none of the above cited combinations of references teach or suggest, *a configurable memory comprising a memory portion for storing tag bits and data bits in a single logical line wherein the configurable memory is configured as a cache*, as essentially claimed. Thus, the above-cited references fail to establish a *prima facie* case for obviousness against any of the claimed inventions.

Accordingly, withdrawal of the obviousness rejections is respectfully requested.

All issues raised by the Examiner having been addressed, reconsideration of the rejections and an early and favorable allowance of this case is earnestly solicited.

Respectfully submitted,



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